

AMENDMENT TO THE SPECIFICATION

On page 6, lines 4-24 replace the existing paragraph with the following:

When an operational code is entered into an expander core, the operational code functions to instruct one of the expander cores 104, 106 to go into bypass mode. When an expander core goes into a bypass mode, it operates as a single bit shift register 208, 222. By placing one of the cores in bypass mode, data can be loaded into the other core to perform a desired operation, such as reading data from one of the internal registers 204, 232 to determine the settings of the expander cores, or writing new data to one of the expander cores to change the operation of the expander cores. However, when one of the expander cores 104, 106 is placed in bypass mode, it will function as a single bit shift register 208, 222, and dummy bits must be provided at the proper time in the sequence of bits to ensure that data is properly loaded into the expander core that is not in the bypass mode. For example, if the second core 106 is placed in bypass mode, an initial dummy bit must be supplied to expander core 104. When expander core 104 is placed in bypass mode, a dummy bit must follow the data supplied to expander core 106. As also shown in Figure 2, a multiplexer 214 and expander core 104 generates an output 219 that is applied to the output J-tag port (TDO) 122 of expander core 104. The output 219 is selected from one of the inputs 220 or 216 in response to a control signal 218 that is generated by state machine 206. If expander core 104 is placed in bypass mode, the input signal from the input J-tag port 120 is applied to both the single bit shift register 208 and to the multi-bit shift register 212. However, state machine 206 generates a control signal 218 that is applied to multiplexer 214 to select input 220 to shift data out over the output 219 of multiplexer 214.